In The United States Patent and Trademark Office
On Appeal From The Examiner To The Board
of Patent Appeals and Interferences

In re Application of:	Mark T. McCormack et al.
Serial No.:	09/866,092
Filing Date:	May 23, 2001
Group Art No.:	2815
Confirmation No.:	5484
Examiner:	Eugene Lee
Title:	*Structure and Method for Embedding Components In Multi-Layer Substrates*

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Appeal Brief

Appellants have appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner sent electronically November 26, 2007, finally rejecting Claims 17-24, 26-34 and 36-44, all of which are pending in this case. Appellants filed a Notice of Appeal on January 7, 2008. Appellants respectfully submit this Appeal Brief with the statutory fee of $510.00.

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Real Party In Interest

This application is currently owned by Fujitsu Limited as indicated by an assignment recorded on September 10, 2001, in the Assignment Records of the United States Patent and Trademark Office at Reel 012160, Frame 0905.

Related Appeals and Interferences

There are no known appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision regarding this appeal.

Status of Claims

Claims 17-24, 26-34, and 36-44 are pending in this application and all stand rejected under a Final Office Action sent electronically November 26, 2007. Appellants present Claims 17-24, 26-34, and 36-44 for appeal. Appendix A shows these claims involved in this appeal.

Status of Amendments

All amendments presented by the Appellants have been entered by the Examiner.

Summary of Claimed Subject Matter

For the convenience of the Board, Appellants provide the following mappings of the claims here on appeal. Appellants do not necessarily identify all portions of the specification and drawings relevant to the recited elements of the claims. Appellants provide the following mapping not to limit the scope of the claims, but to help the Board make a decision on this Appeal.

Independent Claim 17 is directed to a multi-layer printed circuit board having at least one prefabricated, integrated electronic component embedded therein, where the core of the multi-layer printed circuit board is a polymeric circuit board substrate with first and second surfaces (e.g., see, page 3, lines 2 – 4, page 7, lines 2 – 4, ref. nos. 10, 12, 12a, and 12b in Fig. 1, and ref. no. 20 in Fig. 3). An integrated electronic component is prefabricated prior to being securely attached in a cavity in the first surface of the polymeric substrate (e.g., see page 3, lines 4 – 6, page 7, lines 26 – 30, ref. no. 20 in Figs. 3 and 13 and ref. no. 24 in Fig. 12). A dielectric layer is disposed on the first substrate surface and over the integrated electronic component, and a metallic layer is disposed on the dielectric layer (e.g., see page 3, lines 5 – 7, page 8, lines 13 – 21, ref. nos. 30 and 32 in Fig. 4, and ref. nos. 40 and 42 in Figs. 5 and 6). An electrically conductive via passes through the dielectric layer in contact with the metallic layer and a second dielectric layer is disposed over the via and the metallic layer (e.g., see page 3, lines 8 – 10, page 8, lines 12 – 15 and 22 – 31, ref. nos. 46 and 50 in Fig. 6, and ref. nos. 60 and 64 in Fig. 8). A second electrically conductive via extends at one location through the first and second dielectric layers and is electrically coupled to the integrated electronic component (e.g., see page 3, lines 10 – 12, page 8, lines 16 – 19, and ref. no. 70 in Fig. 9).

Independent Claim 40 is directed to a multi-layer printed circuit board, where the core of the multi-layer printed circuit board is a polymeric circuit board substrate, having a prefabricated capacitor disposed in a cavity in the substrate, where the capacitor has a contact pad (e.g., see page 3, lines 2 – 6, page 7, lines 2 – 4 and 26 – 30, page 8, lines 1 - 5, ref. nos. 10 and 12 in Fig. 1, ref. nos. 20 and 26 in Fig. 3, and ref. no. 24 in Fig. 12). A dielectric layer is disposed on the substrate and over the capacitor, and a metallic layer is disposed on the dielectric layer (e.g., see page 3, lines 5 – 7, page 8, lines 13 – 21, ref. nos. 30 and 32 in

Fig. 4, and ref. nos. 40 and 42 in Figs. 5 and 6). An electrically conductive via passes through the dielectric layer in contact with the contact pad and a second dielectric layer is disposed over the via and the metallic layer (e.g., see page 3, lines 8 – 10, page 8, lines 12 – 15 and 22 – 31, ref. nos. 46 and 50 in Fig. 6, and ref. nos. 60 and 64 in Fig. 8). A second electrically conductive via extends at one location through the first and second dielectric layers and is electrically coupled to the capacitor (e.g., see page 3, lines 10 – 12, page 8, lines 16 – 19, and ref. no. 70 in Fig. 9).

Independent Claim 44 is directed to a multi-layer printed circuit board, where the core of the multi-layer printed circuit board is a polymeric circuit board substrate with opposing first and second sides, having a prefabricated electronic component disposed in a cavity in the first side of the substrate, where the prefabricated electronic component has a contact pad (e.g., see page 3, lines 2 – 6, page 7, lines 2 – 4 and 26 – 30, page 8, lines 1 – 5, ref. nos. 10 and 12 in Fig. 1, ref. nos. 20 and 26 in Fig. 3, and ref. no. 24 in Fig. 12). A dielectric layer is disposed on the first side of the substrate and over the prefabricated electronic component, and a metallic layer is disposed on the dielectric layer (e.g., see page 3, lines 5 – 7, page 8, lines 13 – 21, ref. nos. 30 and 32 in Fig. 4, and ref. nos. 40 and 42 in Figs. 5 and 6). An electrically conductive via passes through the dielectric layer in contact with the contact pad and a second dielectric layer is disposed over the via and the metallic layer (e.g., see page 3, lines 8 – 10, page 8, lines 12 – 15 and 22 – 31, ref. nos. 46 and 50 in Fig. 6, and ref. nos. 60 and 64 in Fig. 8). A second electrically conductive via extends at one location through the first and second dielectric layers (e.g., see page 3, lines 10 – 12, page 8, lines 16 – 19, and ref. no. 70 in Fig. 9). A third dielectric layer is disposed on the second side of the substrate and a patterned metallic layer is disposed on the third dielectric layer (e.g., see page 9, lines 12 – 30, and ref. nos. 32, 94 and 98 in Fig. 9).

Grounds of Rejection to be Reviewed on Appeal

Appellants request that the Board review the Examiner's rejection of 17-24, 26-34, 36-44, and 37-42.

Argument

I. The Examiner's Rejection of Claims 17, 33, 34, 38, and 39 is Improper

The Examiner rejects Claims 17, 33, 34, 38, and 39 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,154,366 issued to Ma et al. ("*Ma*") in view of U.S. Patent No. 5,866,952 issued to Wojnarowski et al. ("*Wojnarowski*"), and further in view of U.S. Patent No. 6,861,284 issued to Higashi et al. ("*Higashi*").

Independent Claim 17 of the present application, as amended, recites the following limitations:

> A multi-layer printed circuit board having at least one prefabricated integrated electronic component embedded therein comprising:
>
> a polymeric circuit board substrate having a first substrate surface, ~~and~~ a second substrate surface, and a cavity formed in said first substrate surface;
>
> a first integrated electronic component, where said first integrated electronic component is prefabricated prior to being securely attached in the cavity;
>
> a first dielectric layer disposed on said first substrate surface and over said first integrated electronic component;
>
> a metallic layer disposed on said first dielectric layer;
>
> an electrically conductive first via passing through said first dielectric layer in contact with said metallic layer;
>
> a second dielectric layer disposed over said first via and over said metallic layer; and
>
> a second electrically conductive via extending at one location through said first and second dielectric layers and electrically coupled to said first integrated electronic component.

To establish a *prima facie* case of obviousness, the references must teach or suggest all elements of the rejected claims and it must have been obvious to one of ordinary skill in the art at the time of invention to combine or modify the references. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 82 U.S.P.Q.2d 1385 (2007); *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Appellants respectfully submit that the cited references do not teach or suggest all elements of the rejected claims and that it would not have been obvious to one of ordinary skill in the art to combine these references in the manner proposed by the Examiner.

As noted above, Claim 17 recites "a polymeric circuit board substrate having a first substrate surface, a second substrate surface, and a cavity formed in said first substrate surface." However, Appellants respectfully submit that the proposed combination of references does not disclose, teach or suggest a polymeric circuit board substrate having a cavity formed in a first substrate surface. The Final Office Action, as with the previous Office Actions, does not describe or even mention what feature of *Ma* allegedly teaches this limitation. Appellants believe that it is clear that *Ma* does not disclose a substrate having a cavity formed in the substrate. *Ma* merely shows an IC chip that is mounted on a flexible wiring interconnect, referred to in the patent as a "flex component." The chip is then encapsulated with an encapsulant, and additional wiring layers may be added onto the flex component. *Ma* is principally directed to the use of moisture barriers surrounding the chip. *Ma* does not show a cavity formed in a substrate in which a prefabricated component is mounted. On the contrary, in *Ma*, a component is surrounded, after having already been connected to a flex component, with an encapsulating material. This technique is much different than securing a prefabricated component in a cavity that has been formed in a substrate. Clearly, the encapsulation material is not a substrate as claimed and does not have a cavity formed therein.

In the Response to Arguments section of the Final Office Action, the Examiner appears to argue that "a cavity formed in said first substrate surface" is a product-by-process limitation and that such a limitation is "directed to the product, per se, no matter how actually made." However, Applicant is not arguing about the process by which the claimed cavity is made. Applicants position is simply that there is no cavity disclosed in *Ma*. The cavity is required structure of the claim, and the Examiner has continually failed to point out where such a cavity is disclosed in *Ma*. Applicants discussion regarding how the device in *Ma* is constructed is simply to point out that there is never a cavity present at any step in the manufacture of the device of *Ma*, as shown in its figures.

Furthermore, the Final Office Action contends that, although *Ma* does not disclose a polymeric substrate, it would have been obvious to combine the teachings of *Wojnarowski* with those of *Ma*. In particular, the Office Action asserts that it would have been obvious to use *Wojnarowski's* substrate molding material as the encapsulation material of *Ma* (which the

Office Action alleges is the claimed substrate). The Office Action states that this would have been obvious "to have the circuit board substrate being polymeric in order to have a material that adequately supports a die in a substrate form, and any overlaying materials wherein the material is not prone to cracking." Appellants respectfully disagree with the Examiner.

As an initial matter, *Ma* discloses that the encapsulation material 112 (again, which the Office Action incorrectly alleges is the claimed substrate) can be a plastic material (a polymer). *See Ma, Column 3, lines 3-5.* Therefore, while Appellants disagree with the Office Action's assertion that the encapsulation material is the recited substrate, Appellants do not understand why the Office Action uses the teachings of *Wojnarowski* to suggest a supposedly obvious modification to the material of which the encapsulation material is comprised (when it is already disclosed in *Ma* that the encapsulation material may be a polymer). It would appear that the Examiner sees the weakness in the assertion that encapsulation material 112 is a substrate as claimed, and thus proceeds to bring in the teachings of *Wojnarowski* for a teaching of a substrate. However, Appellants submit that the Office Action has not provided a sufficient basis for combining the teachings of *Ma* with those of *Wojnarowski*. There is no disclosure or suggestion in *Ma* that the encapsulation material 112 serves to support the die and thus there is no suggestion to modify *Ma* such that the encapsulation material should be modified "in order to have a material that adequately supports a die in substrate form." Furthermore, assuming for the sake of argument that some other element, such as the flex component 102 of *Ma*, is deemed to be a substrate (although not argued by the Office Action since this flex component also clearly does not have a cavity), there is also no suggested provided to modify *Ma* such that the flex component is polymeric (and even if there was, it would be irrelevant since the flex component 102 does not have a cavity, as required by Claim 17).

In *KSR Int'l Co. v. Teleflex Inc.*, the Supreme Court clarified the appropriate standard to use when determining obviousness. "The [obviousness] analysis is objective: 'Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject

matter is determined.'" *Id.* (citing *Graham v. John Deere*, 383 U.S. 1, 17-18, 148 U.S.P.Q. 459 (1966)).

A "principal reason for declining to allow patents for what is obvious" is to prevent individuals from obtaining a patent "for a combination which only unites old elements with no change in their respective functions." *Id.* However, the Supreme Court clarified that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *Id.* "[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* While not a rigid test, a showing of a "teaching, suggestion, or motivation" to combine or modify prior art provides helpful insight in determining whether it would have been obvious to combine references. *Id.* "A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning." *Id.* (citing *Graham*, 383 U.S. at 36).

In the present case, Appellants respectfully contend that the Examiner provides no indication that the claims "only unite old elements with no change in their respective functions." Furthermore, the Examiner has not shown a teaching, suggestion, or motivation to combine *Ma* and *Wojnarowski* in the manner suggested. Appellants respectfully submit that the Supreme Court is clear that the type of argument provided in the present Office Action is insufficient to establish obviousness: "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). The Office Action has simply not presented any "articulated reasoning with some rational underpinning" that it would have been obvious to make the proposed combination. For at least these reasons, Appellants respectfully submit that the Office Action fails to present a *prima facie* case of obviousness. Therefore, Appellants request that the rejection of Claim 17, as well as the rejections of those claims that depend from Claim 17 (including Claims 33, 34, 38, and 39), be withdrawn.

II. The Examiner's Rejection of Claims 18, 20-23, 27, 30, 36, 40, 41, and 43 is Improper

Furthermore, the Examiner rejects Claims 18, 20-23, 27, 30, 36, 40, 41, and 43 under 35 U.S.C. § 103(a) as being unpatentable over *Ma* in view of *Wojnarowski* in view of *Higashi*, as applied to Claims 17, 33, 34, 38, and 39, and further in view of U.S. Patent No. 5,565,706 issued to Miura et al. ("*Miura*").

Each of Claims 18, 20-23, 27, 30, and 36 depend from Claim 17 (either directly or via an intervening claim). Therefore, these claims are at least allowable for the reasons discussed above. Thus, Appellants respectfully request reconsideration and allowance of these claims.

Independent Claim 40 (and dependent Claims 41 and 43, due to their dependence on Claim 40) recites "a polymeric circuit board substrate having a cavity formed therein a prefabricated capacitor disposed in ~~a~~ the cavity in said substrate." This limitation is similar to the limitations discussed above with respect to Claim 17. Therefore, Claims 40, 41 and 43 are at least allowable for the reasons discussed above. Thus, Appellants respectfully request reconsideration and allowance of these claims.

In addition, Appellants respectfully submit that Claim 18 is also allowable because the Examiner has not shown a teaching, suggestion, or motivation to combine *Miura* with the other cited references in the manner suggested. As the Final Office Action notes, the combination of *Ma* in view of *Wojnarowski* in view of *Higashi* does not disclose "a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface," as recited in Claim 18. However, the Final Office Action states that such a limitation would be obvious in light of the combination of these references with *Miura*. Specifically, the Final Office Action states that "it would have been obvious" to have the limitation claimed "in order to include external connections to the substrate." However, Appellants respectfully submit that there is no suggestion or motivation to provide "external connections" to the die 106 of *Ma* through the disclosed encapsulation material 112. In fact, that would be against the teachings of *Ma* that material 112 *encapsulates* the die

(at least on the side on which it is applied). The Office Action has simply not presented any "articulated reasoning with some rational underpinning" that it would have been obvious to make the proposed combination. For at least this additional reason, Appellants respectfully submit that the Office Action fails to present a *prima facie* case of obviousness with respect to Claim 18.

III. The Examiner's Rejection of Claim 19 is Improper

The Examiner also rejects Claim 19 under 35 U.S.C. § 103(a) as being unpatentable over *Ma* in view of *Wojnarowski* in view of *Higashi*, as applied to Claims 17, 33, 34, 38, and 39, and further in view of U.S. Patent No. 5,739,188 issued to Desai ("*Desai*").

Claim 19 depends from Claim 17, and thus it is allowable at least for the reasons discussed above in conjunction with Claim 17. Additionally, the Examiner has not shown sufficient motivation to combine *Desai* with *Ma* in view of *Wojnarowski* in view of *Higashi* to disclose that the circuit board substrate recited in Claim 17 "comprises a multi-layer core substrate comprising at least two polymeric layers." First, *Desai* is in a wholly different art than the references with which it has been combined. *Desai* teaches a thermoplastic polymer compound and a method of processing that compound. It does not relate to the formation or processing of polymeric substrates for circuit boards or even to the field of electronic components generally, nor does the reference provide that any of its teachings may be applicable to the formation of a circuit board. *Desai* is primarily concerned with improving the processing stability of thermoplastic polymers and improving their flow characteristics. There is no indication that the problems addressed by *Desai* have any relation to those in *Ma*, *Wojnarowski*, or *Higashi*, or to the present application.

Second, the Examiner has stated as the motivation to combine these references the protection of the substrate. However, the Examiner has provided no support for that line of reasoning. There must be some basis in the references or the art as a whole that provides a teaching, suggestion or motivation to combine. Here, *Desai* teaches a multi-layered polymer product where a core layer is covered by a cap layer not for the protection of the core layer, as suggested by the Examiner, but to hide the imperfections in the core layer. *Desai*, *Column*

3, lines 26-37. Similarly, there is no teaching in any of the references with which *Desai* was combined that suggests the motivation cited by the Examiner.

For at least this additional reason, Appellants respectfully submit that the Office Action fails to present a *prima facie* case of obviousness with respect to Claim 19. Appellants thus respectfully request reconsideration and allowance.

IV. The Examiner's Rejection of Claims 24, 26, 28, 29, 31, 32, and 44 is Improper

In addition, the Examiner also rejects Claims 24, 26, 28, 29, 31, 32, and 44 under 35 U.S.C. § 103(a) as being unpatentable over *Ma* in view of *Wojnarowski* in view of *Higashi*, in view of *Miura* as applied to Claims 18, 20-23, 27, 30, 36, 40, 41, and 43, and further in view of U.S. Patent No. 5,241,456 issued to Marcinkiewicz et al. ("*Marcinkiewicz*").

Each of Claims 24, 26, 28, 29, 31 and 32 depend from Claim 17 (either directly or via an intervening claim). Therefore, these claims are at least allowable for the reasons discussed above. Thus, Appellants respectfully request reconsideration and allowance of these claims.

Independent Claim 44 recites "a polymeric circuit board substrate having opposing first and second sides" and "a prefabricated electronic component disposed in a cavity formed in said first side of said substrate." This limitation is similar to the limitations discussed above with respect to Claim 17. Therefore, Claim 44 is at least allowable for the reasons discussed above. Thus, Appellants respectfully request reconsideration and allowance of Claim 40.

V. The Examiner's Rejection of Claims 37 and 42 is Improper

In addition, the Examiner also rejects Claims 37 and 42 under 35 U.S.C. § 103(a) as being unpatentable over *Ma* in view of *Wojnarowski* in view of *Higashi*, in view of *Miura* as applied to Claims 18, 20-23, 27, 30, 36, 40, 41, and 43, and further in view of U.S. Patent No. 5,953,619 issued to Miyazawa et al. ("*Miyazawa*").

Claims 37 and 42 depend from Claims 17 and 40, respectively. Therefore, these claims are at least allowable for the reasons discussed above. Thus, Appellants respectfully request reconsideration and allowance of these claims.

Conclusion

Appellants have demonstrated that the present invention, as claimed, is clearly distinguishable over the prior art cited by the Examiner. Therefore, Appellants respectfully request the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

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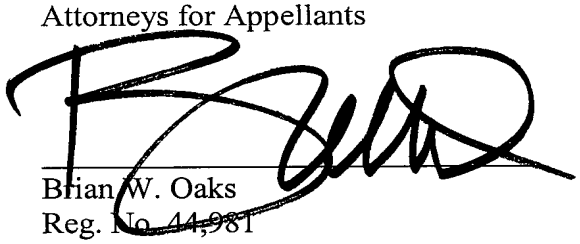
Respectfully submitted,

BAKER BOTTS L.L.P.
Attorneys for Appellants



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Appendix A: Claims on Appeal

1–16 (Cancelled)

17. (Previously Presented) A multi-layer printed circuit board having at least one prefabricated integrated electronic component embedded therein comprising:

a polymeric circuit board substrate having a first substrate surface, a second substrate surface, and a cavity formed in said first substrate surface;

a first integrated electronic component, where said first integrated electronic component is prefabricated prior to being securely attached in the cavity;

a first dielectric layer disposed on said first substrate surface and over said first integrated electronic component;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said metallic layer;

a second dielectric layer disposed over said first via and over said metallic layer; and

a second electrically conductive via extending at one location through said first and second dielectric layers and electrically coupled to said first integrated electronic component.

18. (Previously Presented) The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface.

19. (Previously Presented) The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate comprising at least two polymeric layers.

20. (Previously Presented) The multilayer printed circuit board of Claim 17 wherein said first via extends at least from said first substrate surface to said second substrate surface.

21. (Previously Presented) The multilayer printed circuit board of Claim 18 wherein said first via extends at least from said first substrate surface to said second substrate surface.

22. (Previously Presented) The multilayer printed circuit board of Claim 18 wherein said first metallic layer is patterned to expose a portion of said first substrate surface, and said cavity is formed in the exposed portion of said first substrate surface.

23. (Previously Presented) The multilayer printed circuit board of Claim 18 wherein said second metallic layer is patterned to expose a portion of said second substrate surface.

24. (Original) The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

25. (Cancelled)

26. (Previously Presented) The multilayer printed circuit board of Claim 24 wherein said second integrated electronic component is disposed in a cavity formed in said exposed portion of said second substrate surface.

27. (Previously Presented) The multilayer printed circuit board of Claim 18 wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

28. (Previously Presented) The multilayer printed circuit board of Claim 24 wherein said second integrated electronic component comprises a conductive pad contacting said second metallic layer.

29. (Previously Presented) The multilayer printed circuit board of Claim 26 wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

30. (Original) The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

31. (Previously Presented) The multilayer printed circuit board of Claim 24 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

32. (Original) The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

33. (Original) The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

34. (Original) The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed on said second dielectric layer.

35. (Cancelled)

36. (Previously Presented) The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is a capacitor.

37. (Previously Presented) The multilayer printed circuit board of Claim 36 wherein said capacitor comprises a petrovskite capacitance material.

38. (Previously Presented) The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

39. (Previously Presented) The multilayer printed circuit board of Claim 38 wherein said first prefabricated integrated electronic component is fabricated at a temperature of greater than about 600°C.

40. (Previously Presented) A multi-layer printed circuit board comprising:

a polymeric circuit board substrate having a cavity formed therein a prefabricated capacitor disposed in the cavity in said substrate, said capacitor having a contact pad;

a first dielectric layer disposed on said substrate and over said capacitor;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad;

a second dielectric layer disposed over said first via and over said metallic layer; and

a second electrically conductive via extending at one location through said first and second dielectric layers and electrically coupled to said capacitor.

41. (Previously Presented) The multi-layer printed circuit board of claim 40, comprising a plurality of cavities and a plurality of capacitors.

42. (Previously Presented) The multi-layer printed circuit board of claim 40 wherein said capacitor comprises a petrovskite capacitance material.

43. (Previously Presented) The multi-layer printed circuit board of claim 40 wherein said capacitor is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

44. (Previously Presented) A multi-layer printed circuit board comprising:

a polymeric circuit board substrate having opposing first and second sides;

a prefabricated electronic component disposed in a cavity formed in said first side of said substrate, said prefabricated electronic component having a contact pad;

a first dielectric layer disposed on said first side of said substrate and over said prefabricated electronic component;

a first patterned metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad;

a second dielectric layer disposed over said first via and over said metallic layer;

a second electrically conductive via extending at one location through said first and second dielectric layers;

a third dielectric layer disposed on said second side of said substrate; and

a second patterned metallic layer disposed on said third dielectric layer.

Appendix B: Evidence

NONE

Appendix C: Related Proceedings

NONE